Computer Architecture Objective Type Questions With Answers

Computer Architecture Objective Type Questions With Answers Ace Your Computer Architecture Exam Objective Questions and Answers Cracking the computer architecture exam can seem daunting but fear not This comprehensive guide will equip you with the essential knowledge and understanding of fundamental concepts presented through objective questions and their detailed explanations Lets Dive In 1 Instruction Set Architecture ISA What does ISA define a The organization of the CPU b The physical implementation of the CPU c The set of instructions a CPU can execute d The memory management scheme Answer c The Instruction Set Architecture ISA defines the set of instructions that a CPU can execute along with their formats and operands Which of the following is NOT a characteristic of a RISC Reduced Instruction Set Computing architecture a Simple instructions b Fixedlength instructions c Large number of instructions d Pipelined execution Answer c RISC architectures prioritize simplicity and efficiency characterized by a limited set of instructions compared to CISC Complex Instruction Set Computing 2 CPU Components What is the primary function of the ALU Arithmetic Logic Unit a Store data b Perform arithmetic and logical operations 2 c Manage memory access d Control program flow Answer b The ALU is responsible for executing arithmetic addition subtraction etc and logical AND OR NOT operations Which component is responsible for fetching instructions from memory a ALU b Control Unit c Registers d Program Counter Answer d The Program Counter PC holds the address of the next instruction to be fetched from memory 3 Memory Organization What is the purpose of a cache memory a Store frequently used data for faster access b Manage the allocation of physical memory c Provide a large storage space for data d Implement virtual memory Answer a Cache memory acts as a temporary storage area for frequently accessed data enabling faster retrieval compared to accessing main memory Which memory addressing mode allows the address of the operand to be calculated using a base address and an offset a Register addressing b Immediate addressing c Direct addressing d Indexed addressing Answer d Indexed addressing utilizes a base address and an offset to calculate the actual memory address of the operand 4 Memory Hierarchy Which level of the memory hierarchy is typically the fastest but also the smallest a Main memory b Cache memory c Secondary storage 3 d Registers Answer d Registers are the fastest level in the memory hierarchy offering the quickest access times but with limited storage capacity What is the principle behind the concept of locality of reference a Data is accessed randomly b Data is accessed sequentially in a predictable pattern c Data is accessed in a blockbyblock manner d Data is accessed in a hierarchical order Answer b The principle of locality of reference states that programs tend to access data and instructions in a localized manner either spatially nearby addresses or temporally repeated access in a short time period 5 Pipelining and Parallelism What is the purpose of pipelining in CPU design a Reduce the number of instructions executed b Increase the clock speed c Overlap the execution of multiple instructions d Implement a multicore processor Answer c Pipelining allows multiple instructions to be processed simultaneously in different stages increasing the overall execution speed What type of parallelism involves splitting a task into smaller independent parts that can be executed concurrently on multiple processors a Instructionlevel parallelism b Datalevel parallelism c Threadlevel parallelism d All of the above Answer b Datalevel parallelism focuses on exploiting parallelism at the level of data operations typically by dividing a large dataset into smaller chunks that can be processed concurrently 6 InputOutput IO Which IO technique allows the CPU to perform other tasks while waiting for IO operations to complete a Programmed IO 4 b Interruptdriven IO c Direct memory access DMA d All of the above Answer b Interruptdriven IO allows the CPU to continue processing other tasks while an IO device handles the transfer of data What is the purpose of a device driver a Communicate with the user b Manage the communication between the CPU and an IO device c Store data for the IO device d Handle memory allocation Answer b A device driver acts as a software interface between the CPU and an IO device enabling communication and data transfer 7 Operating System and Memory Management What is the primary role of an operating system a Manage hardware resources b Provide a user interface c Execute applications d All of the above Answer d An

operating system acts as the intermediary between the hardware and applications managing resources providing a user interface and executing applications Which memory management technique allows a process to be divided into smaller parts which can be loaded and executed in different memory locations a Swapping b Paging c Segmentation d Both b and c Answer d Both paging and segmentation allow a process to be broken down into smaller units enabling efficient memory management and multitasking Paging divides a process into fixedsize pages while segmentation divides it into logical units Conquering the Exam By understanding the fundamental concepts and answering practice questions youll gain confidence in your ability to tackle the computer architecture exam Remember thorough 5 practice and a grasp of the underlying principles are key to success Good luck

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